What is claimed is:

1. A method of fabricating a semiconductor device comprising:

forming a gate oxide layer on a semiconductor substrate;

forming a polysilicon layer on the gate oxide layer;

patterning the gate oxide layer and the polysilicon layer defining polysilicon gates therein;

forming L-shaped nitride spacers adjacent to the polysilicon gates;

forming oxide sidewalls over the L-shaped nitride spacers;

performing an active region implant into active regions and defining channel regions therebetween the active regions below the polysilicon gates;

forming a composite nitride cap over the device;

performing a rapid thermal anneal that alters a dopant profile of the channel regions.

2. The method of claim 1, wherein the composite nitride cap covers NMOS devices and PMOS devices of the semiconductor device.

3. The method of claim 1, further comprising selectively removing portions of the composite nitride cap thereby exposing PMOS devices of the semiconductor device.

4. The method of claim 1, wherein the composite silicon nitride cap is formed by depositing a relatively thin liner layer over/on the semiconductor device and forming an upper layer on the liner layer.

5 The method of claim 4, wherein the liner layer is comprised of silicon oxide and the upper layer is comprised substantially of nitride.

6. The method of claim 4, wherein the liner layer is comprised of only nitride.

7. The method of claim 4, wherein the liner layer is comprised of nitride and the upper layer is comprised of oxide.

8. The method of claim 4, wherein the liner layer is comprised of oxynitride and the upper layer is comprised of nitride.

9. The method of claim 4, wherein the liner layer is formed with a thickness of less than about 50 to 100 Angstroms and the upper layer is formed with a thickness of about 800 Angstroms.

10. The method of claim 4, wherein the composite silicon nitride cap has a hydrogen concentration of about great than 15%.

11 The method of claim 1, wherein the composite nitride cap is at least partially formed by depositing nitride via a rapid thermal chemical vapor deposition process at about 500 degrees Celsius.

12. The method of claim 1, wherein the composite nitride cap is at least partially formed by depositing nitride via a plasma enhanced chemical vapor deposition process performed at about 300 to 350 degrees Celsius.

13. The method of claim 1, wherein performing the rapid thermal anneal comprises causing p-type dopants to segregate out of an interface at the channel regions thereby altering the dopant profile for the channel region to create a retrograde profile.

14. The method of claim 1, wherein the L-shaped nitride spacers are formed with bis-tertiary-butyl-amino-silane thereby yielding different etch rates for the L-shaped spacers and the composite nitride cap after annealing process.

15. The method of claim 1, further comprising removing remaining portions of the composite nitride cap.

16. The method of claim 1, further comprising removing remaining portions of the composite nitride cap via combinations of wet etch and/or plasma etch process.

17. The method of claim 1, wherein the channel regions are subject to dopant profile modification such that NMOS transistor current drive is increased by at least 10 percent.

18. The method of claim 15, wherein a relatively thin oxide layer is not removed from at least a portion of the semiconductor device.

19. The method of claim 1, further comprising forming salicide regions on the polysilicon gates and the active regions.

20. A method of fabricating a composite nitride cap comprising:

providing an NMOS semiconductor device having active regions, a channel region and a polysilicon gate;

forming a liner layer over at least a portion of the semiconductor device; and

forming an upper layer on the liner layer wherein the upper layer is substantially thicker than the liner layer and is comprised substantially of nitride.

21. The method of claim 20, further comprising causing dopants to segregate out of an Si/SiO2 interface in the channel region during an annealing process.

22. The method of claim 18, wherein the liner layer is less than about 100 Angstroms and the upper layer is about 800 Angstroms.

23. The method of claim 22, wherein the sidewalls formed are comprised of silicon oxide and nitride.

24. The method of claim 22, wherein the sidewalls formed are comprised substantially of nitride.